

**WHAT IS CLAIMED IS:**

1. A vector controller for a polyphase synchronous  
2 rectifier, comprising:

3 an input line voltage detector configured to detect voltages  
4 on at least two rectifier input lines and produce therefrom a  
5 neutral excursion vector; and

6 a neutral excursion compensator, coupled to said input line  
7 voltage detector, that applies said neutral excursion vector to a  
8 partially compensated drive vector to yield an excursion-  
9 compensated drive vector suitable for generation of excursion-  
10 compensated pulse-width modulated drive signals for said  
11 synchronous rectifier.

2. The controller as recited in Claim 1 further comprising  
2 an input line current detector configured to detect currents on at  
3 least two of said rectifier input lines and produce therefrom an  
4 uncompensated drive vector.

3. The controller as recited in Claim 2 further comprising:

2 an output voltage detector configured to detect a bus voltage  
3 of said synchronous rectifier and produce therefrom a DC bus  
4 voltage; and

5 a current control block, coupled to said output voltage  
6 detector, that applies a reference current vector based on said DC  
7 bus voltage to said uncompensated drive vector to yield said  
8 partially compensated drive vector.

4. The controller as recited in Claim 1 further comprising  
2 a zero-crossing detector configured to detect a phase on one of  
3 said at least two rectifier input lines and produce therefrom a  
4 zero-crossing signal for said input line voltage detector.

5. The controller as recited in Claim 4 wherein said zero-  
2 crossing detector further provides said zero-crossing signal for an  
3 input line current detector.

6. The controller as recited in Claim 1 further comprising  
2 a 2-3 transform that transforms said excursion-compensated drive  
3 vector into signals suitable for a pulse-width modulated drive  
4 signal generator.

7. The controller as recited in Claim 1 further comprising  
2 a pulse-width modulated drive signal generator configured to  
3 generate said excursion-compensated pulse-width modulated drive  
4 signals for said synchronous rectifier.

8. A method of vector-controlling a polyphase synchronous  
2 rectifier, comprising:  
3 detecting voltages on at least two rectifier input lines;  
4 producing therefrom a neutral excursion vector; and  
5 applying said neutral excursion vector to a partially  
6 compensated drive vector to yield an excursion-compensated drive  
7 vector suitable for generation of excursion-compensated pulse-width  
8 modulated drive signals for said synchronous rectifier.

9. The method as recited in Claim 8 further comprising:  
2 detecting currents on at least two of said rectifier input  
3 lines; and  
4 producing therefrom an uncompensated drive vector.

10. The method as recited in Claim 9 further comprising:  
2 detecting a bus voltage of said synchronous rectifier;  
3 producing therefrom a DC bus voltage vector; and  
4 applying a reference current vector based on said DC bus  
5 voltage to said uncompensated drive vector to yield said partially  
6 compensated drive vector.

11. The method as recited in Claim 8 further comprising:

2 detecting a phase on one of said at least two rectifier input  
3 lines; and

4 producing therefrom a zero-crossing signal for said input line  
5 voltage detector.

12. The method as recited in Claim 11 further comprising  
2 further providing said zero-crossing signal for an input line  
3 current detector.

13. The method as recited in Claim 8 further comprising  
2 transforming said excursion-compensated drive vector into signals  
3 suitable for a pulse-width modulated drive signal generator.

14. The method as recited in Claim 8 further comprising  
2 generating said excursion-compensated pulse-width modulated drive  
3 signals for said synchronous rectifier.

15. A three-phase synchronous rectifier, comprising:

2 a plurality of power switches interposing three rectifier  
3 input lines and two rectifier output lines; and

4 a vector controller, including:

5 an input line voltage detector configured to detect  
6 voltages on at least two of said rectifier input lines and  
7 produce therefrom a neutral excursion vector,

8 a neutral excursion compensator, coupled to said input  
9 line voltage detector, that applies said neutral excursion  
10 vector to a partially compensated drive vector to yield an  
11 excursion-compensated drive vector, and

12 a pulse-width modulated drive signal generator configured  
13 to produce excursion-compensated pulse-width modulated drive  
14 signals from said excursion-compensated drive vector and drive  
15 said plurality of drive switches based thereon.

16. The synchronous rectifier as recited in Claim 15 further  
2 comprising an input line current detector configured to detect  
3 currents on at least two of said rectifier input lines and produce  
4 therefrom an uncompensated drive vector.

17. The synchronous rectifier as recited in Claim 16 further  
2 comprising:

3 an output voltage detector configured to detect a bus voltage  
4 across said two rectifier output lines and produce therefrom a DC  
5 bus voltage; and

6 a current control block, coupled to said output voltage  
7 detector, that applies a reference current vector based on said DC  
8 bus voltage to said uncompensated drive vector to yield said  
9 partially compensated drive vector.

18. The synchronous rectifier as recited in Claim 15 further  
2 comprising a zero-crossing detector configured to detect a phase on  
3 one of said three rectifier input lines and produce therefrom a  
4 zero-crossing signal for said input line voltage detector.

19. The synchronous rectifier as recited in Claim 18 wherein  
2 said zero-crossing detector further provides said zero-crossing  
3 signal for an input line current detector.

20. The synchronous rectifier as recited in Claim 15 further  
2 comprising a 2-3 transform that transforms said excursion-  
3 compensated drive vector into signals suitable for said pulse-width  
4 modulated drive signal generator.